Full SoC Power analysis and estimation with end-user software early in the design cycle

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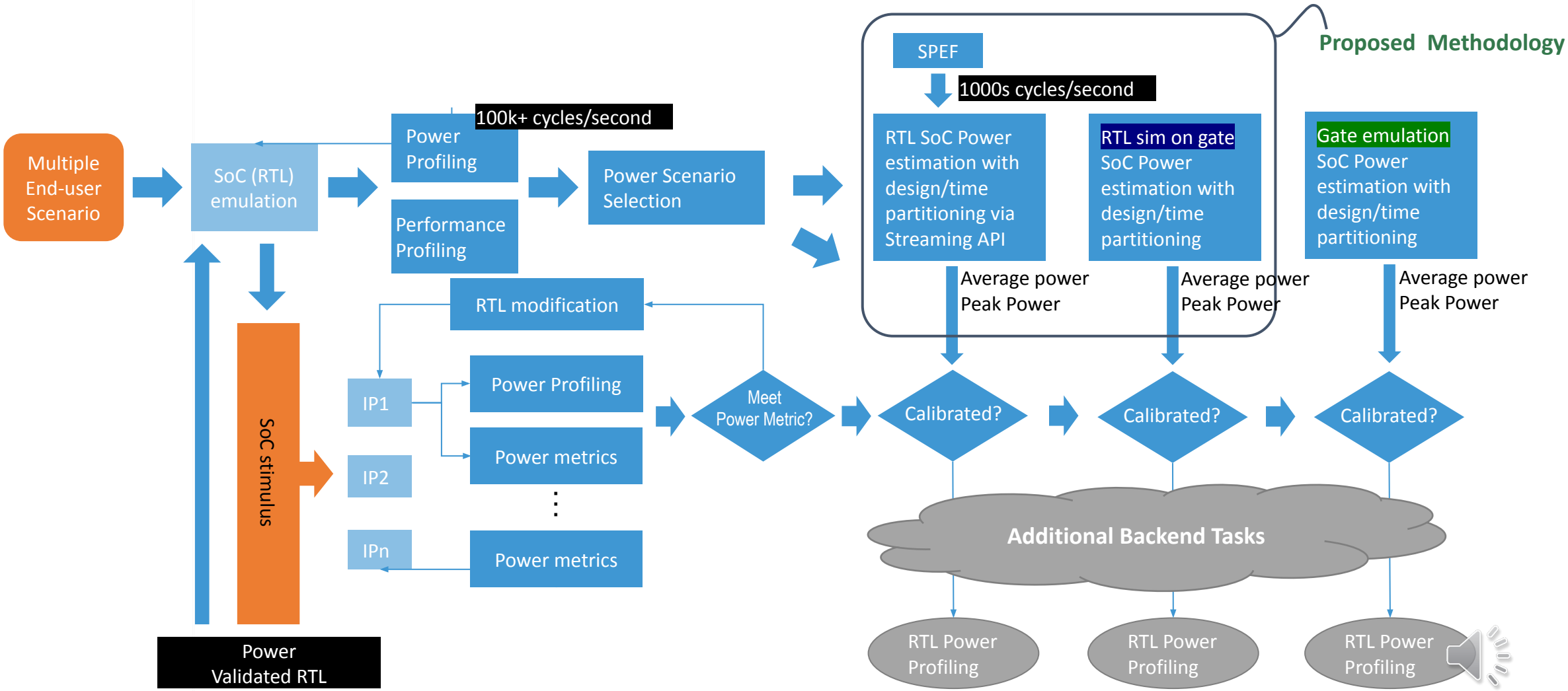
Motivation

- **Failure of Dennard Model**
  - **From middle of 2000, Dennard Model is failure.**
  - **Power analysis through any scaling method is practically impossible**
- **Need enhance estimation accuracy**
  - **Low estimation accuracy due to short analysis period – easy to fall into local minima/maxima**
  - **User scenario/Application based power analysis is required.**
- **Shift-left Paradigm**
  - **Need enough time to resolve power bugs**
  - **Power analysis should be performed on the earliest stage as soon as possible**
- **This paper proposes an advanced power analysis methodology based on user scenarios at early HW design stage**

Proposed Advanced End2End Power Analysis Methodology for Full SoC (1/2)



Proposed Advanced End2End Power Analysis Methodology for Full SoC (2/2)

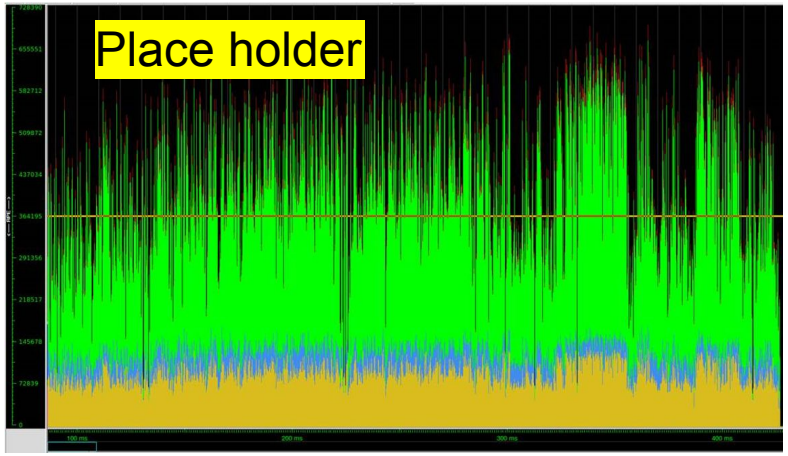
- Key end-user software applications are run on an emulator (which may take billions of cycles)
- All the applications are being profiled for both power and performance
- Stimulus for each IP during application run is captured during in the SoC run
- IP power profile and power metrics are captured with SoC stimulus.
- For each IP, the RTL is modified to improve power efficiency
- RTL modification is validated with fast turnaround time with SoC stimulus
- Power profile and performance profile is used to do power scenario selection

- Power estimation is done for desired power scenarios of full SoC. This is possible via both design and time partitioning.
  The switching activity is streamed to power tool for parallel execution of power calculation while emulation is in progress to reduce time to power
- When gate level netlist and gate mapping file are available, the power estimation is done for the desired power scenarios of full SoC via RTL simulation waveform from emulation with gate level netlist.
- When gate level emulation is available, measure power estimation on gate level emulation.
- For sign off, gate level simulation with SDF is done for providing input to power sign off tool.

Experimental results

Power Profile for Full SoC

Design	Design size (MG)	Design cycles	Emulation exec time	Power Plot and power metric generation
NPU full SoC	500 MG	3.1 billions	2.1 hours	5.8 hours



Veloce – PowerPro flow

Scenario	Emulation time	Design cycles	Emulation exec time	Power value generation	Time to power	Reference
NPU BM	1 ms	8.5 millions	42 mins	3 hours	3 hours 11mins	17 hours
NPU BM	10 ms	85.9 millions	6.4 hours	11 hours	-	

- **Using existed simulation-based power analysis, it was difficult to analyze 1ms power due to low tool performance**
- **By adopting emulation-based power methodology, we can analyze more than 10ms power within a half day. Note that this 10ms is selected based on earlier stage.**

Summary

- End2End Accurate Power Analysis Methodology is Proposed based on User Scenario
  - Allows IP power analysis with full SoC stimulus
  - Enables fast collection of power profile, key power metrics and performance profile.
  - With this profile, Periods which need more detailed power analysis, and IR drop analysis can be detected.
  - Design partition allows to measure SOC level power without area limitation
- Streaming API from Veloce to PowerPro(Siemens)
  - Enable faster power analysis by removing all overhead from the massive disk size.
  - Enable to increase time window for power estimation
  - the possibility of local minima has been reduced by allowing longer analysis of real user scenarios
- In order to analyze accurately without falling into the local minima, it is necessary to find the power projection technique for the representative periods of the user scenario.